

Optical Interconnection Design Innovator

# 800GbE to 800GbE (OSFP to OSFP) Direct Attach Cable P/N: GOS-PC801-XXXC

### Features

- ✓ Hot-plug OSFP form factor with close top heat sink
- ✓ Support 8x 50/100Gb/s PAM4 modulation
- ✓ Commercial case temperature range of 0°C to 70°C
- ✓ 25 AWG ~30 AWG support up to 2m length
- ✓ Contain EEPROM & programmable to customized

## Applications

- Data storage and communication industry
- ✓ Switch / router / HBA
- ✓ Enterprise network
- ✓ Data Center Network
- ✓ Infiniband

## STANDARDS COMPLIANCE

- ✓ IEEE P802.3ck D3.0
- ✓ OSFP MSA HW Rev 4.1
- ✓ ROHS

## Description

Gigalight's GOS-PC801-xxC cable assemblies are effective alternatives to fiber optics. The cable connects data signals from each of the 16 pairs on the single OSFP end to the other OSFP end, each pair operates at data rates of up to 100Gb/s, each OSFP port can be addressed by EEPROM to provide product information, which can be read or write by I2C interface.

Gigalight's GOS-PC801-xxC cable assemblies is compliant with the OSFP-MSA and IEEE 802.3ck, it's a high performance & cost effective I/O solutions for LAN, HPC and SAN. The high speed cable assemblies meet and exceed 800Gigabit Ethernet, InfiniBand EDR /HDR and temperature requirements for performance and reliability.



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# **Absolute Maximum Ratings**

Parameter	Symbol	Min	Мах	Unit
Storage Temperature	Ts	-20	85	°C
Case Operating Temperature	Tc	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

# **Recommended Operating Conditions**

Parameter	Symbol	Min	Typical	Мах	Unit
Operating Case Temperature	Tc	0		70	°C
Baud Rate per Lane (PAM4)	fd		53.125		GBaud/s
Humidity	Rh	5		85	%

# **Mechanical Dimensions**





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OSFP Horizontal Direction				
CABLE GUAGE	DIAMETE R"B"	MIN BEND RADIUS"C"		
26AWG	11MM	55MM	65MM	
25AWG	12MM	60MM	70MM	

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Oppcal Interconnection Design innovator				
OSFP Vertical Direction				
CABLE GUAGE	DIAMETER "B1"	MIN BEND RADIUS"C 1"		
26AWG	8MM	40MM	50MM	
25AWG	9MM	45MM	55MM	

# **Electrical pinout**



Bottom Side (viewed from bottom)



# Electrical pin list and description



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Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground Transmitter Data Non-Inverted	Chall	Input from Host	1	
6	TX4p TX4n	Transmitter Data Non-Inverted	CML-I CML-I	Input from Host Input from Host	3	
7	GND	Ground	CIVIL-I	Input Ironi Host	1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground	CIVIL	mpachonnosc	1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull- up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
	GND RX5n	Ground	Chill O	Outrast to Used	C	
22		Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted Ground	CML-O	Output to Host	3	
24 25	GND RX3n	Receiver Data Inverted	CML-0	Output to Host	1	
25		Receiver Data Inverted	CML-0	Output to Host Output to Host	3	
20	RX3p GND	Ground	CIVIL-O	Output to Host	1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Inverted	CML-0	Output to Host	3	
30	GND	Ground	CIVIL-O	output to host	1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
33	RX2n				Contraction of the second second	4
34		Receiver Data Inverted	CMI-O	Output to Host	3	
34	GND	Receiver Data Inverted Ground	CML-O	Output to Host	3	
	GND				1	
35 36		Ground	CML-0 CML-0 CML-0	Output to Host Output to Host Output to Host	100	
35	GND RX4p	Ground Receiver Data Non-Inverted	CML-0	Output to Host	1 3	
35 36	GND RX4p RX4n	Ground Receiver Data Non-Inverted Receiver Data Inverted	CML-0	Output to Host	1 3 3	
35 36 37	GND RX4p RX4n GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground	CML-O CML-O	Output to Host Output to Host	1 3 3 1	
35 36 37 38	GND RX4p RX4n GND RX6p	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted	CML-O CML-O CML-O	Output to Host Output to Host Output to Host	1 3 3 1 3	
35 36 37 38 39	GND RX4p RX4n GND RX6p RX6n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted	CML-O CML-O CML-O	Output to Host Output to Host Output to Host	1 3 1 3 3 3	
35 36 37 38 39 40	GND RX4p RX4n GND RX6p RX6n GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground	CML-O CML-O CML-O CML-O	Output to Host Output to Host Output to Host Output to Host	1 3 1 3 3 1	
35 36 37 38 39 40 41	GND RX4p RX4n GND RX6p RX6n GND RX8p	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted	CML-O CML-O CML-O CML-O CML-O	Output to Host Output to Host Output to Host Output to Host Output to Host	1 3 1 3 3 1 3 3	
35 36 37 38 39 40 41 42	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8p RX8n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted	CML-O CML-O CML-O CML-O CML-O	Output to Host Output to Host Output to Host Output to Host Output to Host	1 3 1 3 1 3 1 3 3 3	See pin description for required circuit
35 36 37 38 39 40 41 42 43	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground	CML-0 CML-0 CML-0 CML-0 CML-0 CML-0	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host	1 3 1 3 1 3 1 3 1 3 1	
35 36 37 38 39 40 41 42 43 44	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset	CML-0 CML-0 CML-0 CML-0 CML-0 CML-0	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional	1 3 1 3 1 3 3 1 3 3 1 3	for required circuit
35 36 37 38 39 40 41 42 43 44 45 46 47	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data	CML-0 CML-0 CML-0 CML-0 CML-0 CML-0	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host	1 3 1 3 1 3 1 3 1 3 2 2 2 3	
35         36           37         38           39         40           41         42           43         44           45         46           47         48	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional	1 3 1 3 1 3 1 3 1 3 2 2 2 3 1	for required circuit Open-Drain with pull-
35         36           37         38           39         40           41         42           43         44           45         46           47         48           49         49	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host	1 3 3 1 3 1 3 3 1 3 2 2 2 3 3 1 3	for required circuit Open-Drain with pull-
35         36           37         38           39         40           41         42           43         44           45         46           47         48           49         50	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Non-Inverted	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional	1 3 3 1 3 1 3 3 1 3 2 2 2 3 1 3 3 3 3	for required circuit Open-Drain with pull-
35         36           37         38           39         40           41         42           43         44           45         46           47         48           49         50           51         51	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host	1 3 3 1 3 1 3 3 1 3 2 2 2 3 1 3 3 1 3 1	for required circuit Open-Drain with pull-
35         36           36         37           38         39           40         41           42         43           44         45           46         47           48         49           50         51           52         52	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND TX5n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host	1 3 1 3 1 3 1 3 1 3 2 2 2 3 1 3 3 1 3 3 3 1 3 3 3 3 3 3 3 3 3 3 3 3 3	for required circuit Open-Drain with pull-
35         36           36         37           38         39           40         41           42         43           44         45           46         47           48         49           50         51           52         53	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND TX7p GND TX5n TX5p	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted Transmitter Data Inverted	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host	1 3 1 3 1 3 1 3 1 3 2 2 2 3 1 3 1 3 1 3 1 3 3 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 3 3 3 3 3 3 3 3 3	for required circuit Open-Drain with pull-
35         36           36         37           38         39           40         41           42         43           44         45           46         47           48         49           50         51           52         53           54         54	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial Interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host	1 3 1 3 1 3 1 3 1 3 2 2 2 3 1 3 3 1 1 3 1 1 3 1 1 3 1 1 3 1 1 1 1 1 1 1 1 1 1 1 1 1	for required circuit Open-Drain with pull-
35       36       37       38       39       40       41       42       43       44       45       46       47       48       49       50       51       52       53       54       55	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND TX3n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host Input from Host	1 3 1 3 1 3 1 3 1 3 2 2 2 3 1 3 1 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 3 3 3 3 3 3 3 3 3 3	for required circuit Open-Drain with pull-
35         36           36         37           38         39           40         41           42         43           44         45           46         47           48         49           50         51           52         53           54         55           56         56	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND TX3n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Module Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host	1 3 1 3 1 3 1 3 1 3 2 2 2 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 3 3 1 3 3 3 3 3 3 3 3 3 3 3 3 3	for required circuit Open-Drain with pull-
35         36           37         38           39         40           41         42           43         41           42         43           44         45           46         47           48         49           50         51           52         53           54         55           56         57	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND TX3n TX3p GND	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host Input from Host Input from Host	1 3 1 3 1 3 1 3 1 3 2 2 2 3 1 3 1 3 3 1 3 3 1 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 1 3 3 1 1 3 3 1 1 1 1 1 1 1 1 1 1 1 1 1	for required circuit Open-Drain with pull-
35         36           36         37           38         39           40         41           42         43           44         45           46         47           48         49           50         51           52         53           54         55           56         56	GND RX4p RX4n GND RX6p RX6n GND RX8p RX8n GND INT/RSTn VCC VCC SDA GND TX7n TX7p GND TX7n TX7p GND TX5n TX5p GND TX3n	Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Receiver Data Non-Inverted Receiver Data Inverted Ground Module Interrupt / Module Reset +3.3V Power +3.3V Power 2-wire Serial interface data Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Module Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Ground Transmitter Data Inverted Transmitter Data Inverted Ground	CML-O CML-O CML-O CML-O CML-O CML-O Multi-Level LVCMOS-I/O CML-I CML-I CML-I CML-I	Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Output to Host Bi-directional Power from Host Bi-directional Input from Host Input from Host Input from Host Input from Host	1 3 1 3 1 3 1 3 1 3 2 2 2 3 1 3 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 1 3 3 3 3 1 3 3 3 3 3 1 3 3 3 3 3 3 3 3 3 3 3 3 3	for required circuit Open-Drain with pull-



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Part Number		GQD-PC801-XXXC	
Length (meter)	0.5	1	2
Wire gauge (AWG)	30	30	26/25

If length(meter) is decimal, PN should be as GOS-PC801-DXXC.

## **Important Notice**

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by Gigalight before they become applicable to any particular order or contract. In accordance with the Gigalight policy of continuous improvement specifications may change without notice.

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# **Revision History**

Revision	Date	Description
V0	Oct-12-2023	Advance Release.