200GBASE-SR4 QSFP56 Optical Transceiver Module
GQS-MPO201-SR4CZC DSP Version

Features

- ✓ Hot-pluggable QSFP56 form factor
- ✓ Built-in200G PAM4 DSP
- ✓ Supports 212.5Gb/saggregate bit rates
- ✓ Supports 103.125Gb/s aggregate bit rates if required[Note]
- ✓ Low power dissipation <5W
- ✓ RoHS-6 compliant (lead-free)
- ✓ Commercial case temperature rangeof 0°C to 70°C
- ✓ Single 3.3V power supply
- ✓ Maximum link length of 70m onOM3 MMF
  and100m on OM4& OM5 MMF
- ✓ Uncooled 4 channels 850nm VCSEL array
- ✓ 4 channels PIN photo detector array
- ✓ 200GAUI-4 electrical interface
- ✓ Single MPO12 receptacle
- ✓ CMIS V4.0 compliant
- ✓ Built-in digital diagnostic functionality

Applications

- ✓ IEEE 802.3cd 200GBASE-SR4 Ethernet (PAM4)
- ✓ IEEE 802.3bm 100GBASE-SR4 Ethernet (NRZ) [Note1]

Description

Gigalight'sGQS-MPO201-SR4CZ200GE QSFP56Optical Transceivermodules are designed for use in 200Gigabit Ethernet links over OM3/OM4/OM5 multimode fiber. Theyare compliant with the QSFP MSAand with IEEE 802.3cd200GBASE-SR4 specification. Digitaldiagnostics functions are available via the I2C interface as specified by CMIS V4.0. The transceiver is RoHS 2.0 compliantand lead-free perDirective 2011/65/EU.

Note:

Note1:Contact Gigalightformore details.

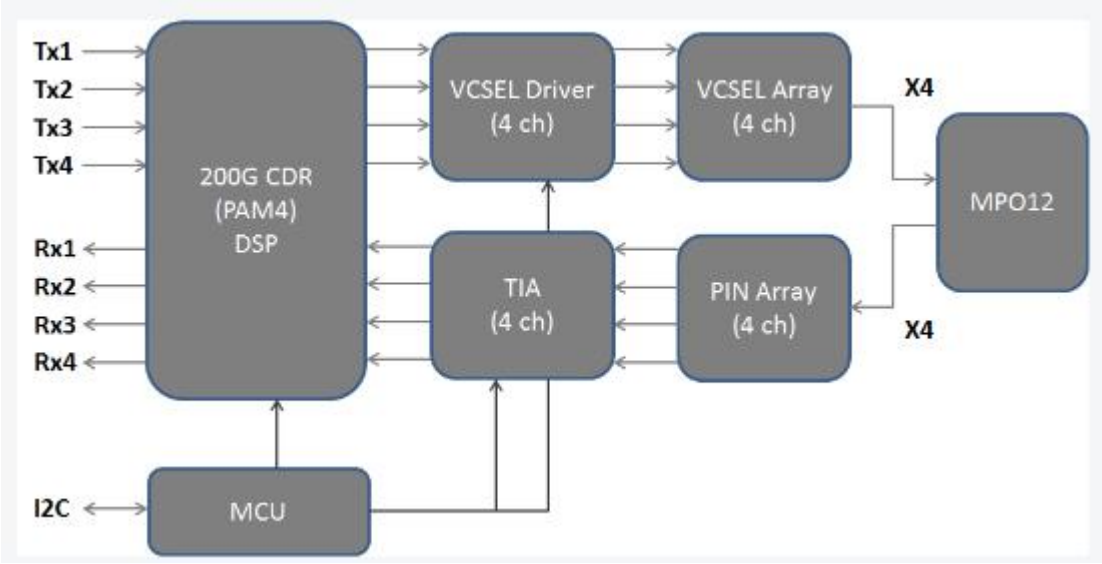

Figure 1. Module Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	V_{cc}+0.3	V
Storage Temperature	T_s	-40	85	ºC
Case Operating Temperature	T_c	0	70	ºC
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case Temperature	T_c	0		70	ºC
Baud Rate per Lane (PAM4)	fd		26.5625		GBaud/s
Humidity	Rh	5		85	%
Power Dissipation	P_m		4.1	4.5	W
Fiber Bend Radius	R_b	3			cm

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude	ΔV_{in}	300		1000	mVpp
Differential Output Voltage Amplitude	ΔV_{out}	300		900	mVpp
Bit Error Rate Note2	BER			2.4E-4	
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V

Output Logic Level High	V_{OH}	V_{cc}-0.5		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Note:

Note2. Compliant with 200GBASE-SR4 electrical specificationin IEEE802.3cd standard.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Center Wavelength	λc	840	850	860	nm
RMS Spectral Width	Δλ			0.6	nm
Average Launch Power (each lane)	P_{out}	-6.5		4	dBm
Outer Optical Modulation Amplitude (each lane)	OMA_{out}	-4.5		3	dBm
Launch power in OMA_{outer} minus TDECQ	P_{tdecq}	-5.9			dBm
Transmitter and dispersion eye closure (each	TDEC			4.5	dB
Average launch power of off transmitter(each	P_{off}			-30	dBm
Outer Extinction Ratio	ER	3			dB
Optical Return Loss Tolerance	ORLT			12	dB
Receiver					
Center Wavelength	λ_c	840	850	860	nm
Damage threshold	Rdam			4	dBm
Average Receive Power (each lane)	Pin	-7.9		4	dBm
Receiver Power (OMA_{outer}) (each lane)	OMA_{out}			3	dBm
Receiver reflectance	Pref			-12	dB
Stressed Receiver Sensitivity (OMA_{outer}) (each lane)	Sens			-3	dBm
Receiver Sensitivity (OMA_{outer}) (each lane) Note3	Sen			-7	dBm
LOS Assert				-10	dBm
LOS De-Assert				-8.5	dBm
LOS Hysteresis		0.5			dB

Note:

Note3. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC

Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground Note5
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground Note5
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground Note5
8	LVTTL-I	MODSEIL	Module Select Note6
9	LVTTL-I	ResetL	Module Reset Note6

10		VCCRx	+3.3V Receiver Power Supply
11	LVCMOS-I	SCL	2-wire Serial interface clock[Note6]
12	LVCMOS-I/O	SDA	2-wire Serial interface data[Note6]
13		GND	Module Ground[Note5]
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground[Note5]
17	CML-O	RX1+	Receiver non-inverted data output
18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground[Note5]
20		GND	Module Ground[Note5]
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground[Note5]
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground[Note5]
27	LVTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTL-O	IntL	Interrupt output, should be pulled up on host board[2]
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTL-I	LPMode	Low Power Mode[Note6]
32		GND	Module Ground[Note5]
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground[Note5]
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground[Note5]

Note:

Note5. Module circuit ground is isolated from module chassis ground within the module.

Note6. Open collector should be pulled up with 4.7K to 10K ohms on host board to a voltage between 3.15V and 3.6V.

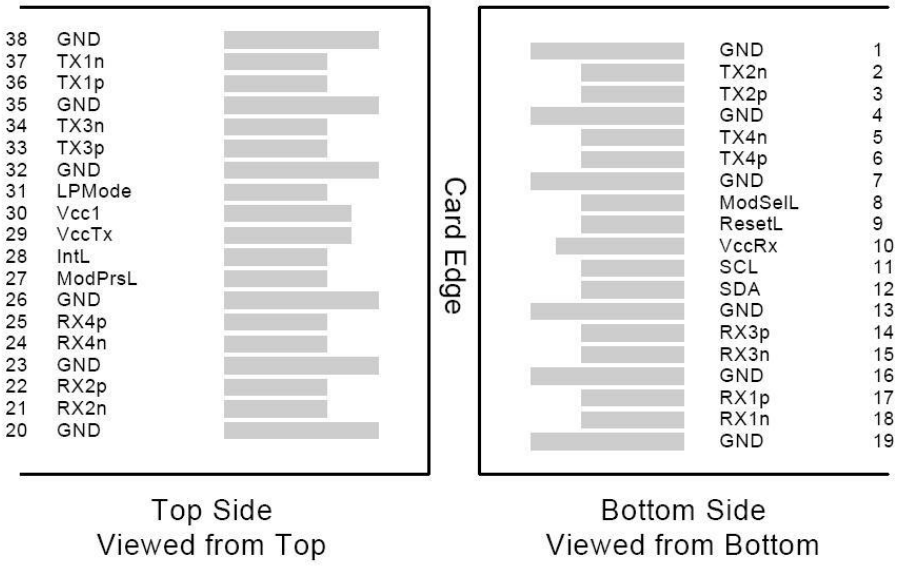

Figure 2. Electrical Pin-out Details

ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is "High", the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Gigalight QSFP28 modules operate in the low power mode (less than 1.5 W power consumption). This pin active high will decrease power consumption to less than 1W.

ModPrsL Pin

ModPrsL is pulled up to Vcc on the host board and grounded in the module. The ModPrsL is asserted "Low" when the module is inserted and deasserted "High" when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to Vcc on the host board.

Power Supply Filtering

The host board should use the power supply filtering shown in Figure 3.

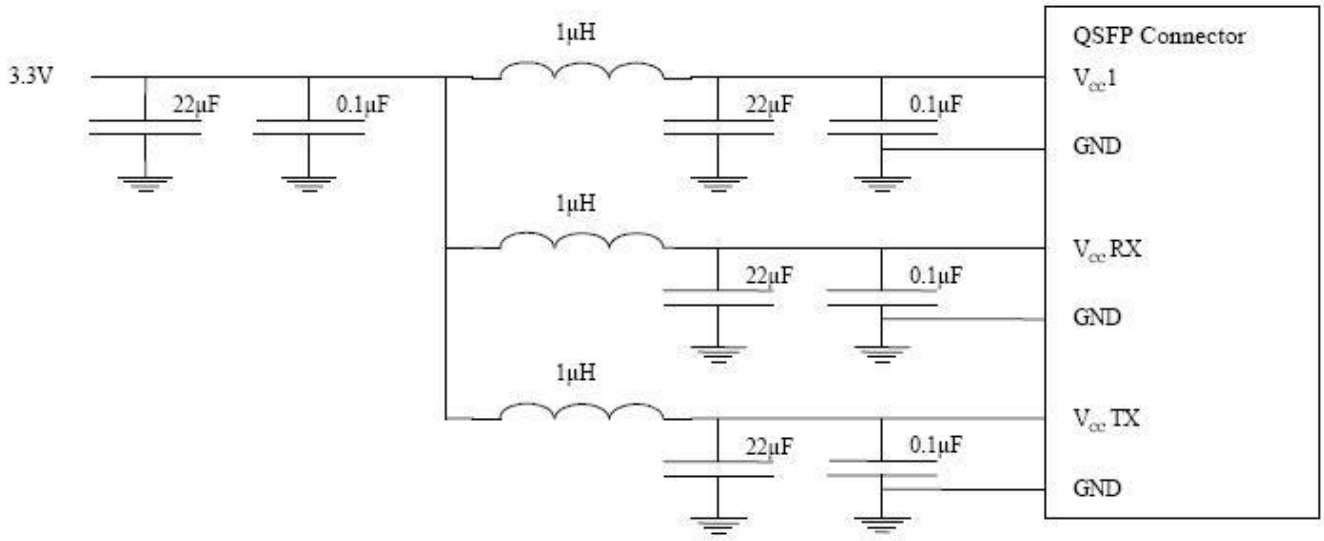

Figure 3. Host Board Power Supply Filtering

Optical Interface Lanes and Assignment

The optical interface port is a male MPO connector.The four fiber positions on the left as shown in Figure 4, with the key up, are used for the optical transmit signals (Channel 1 through 4). The fiber positions on the right are used for the optical receive signals (Channel 4 through 1). The central four fibers are physically present.

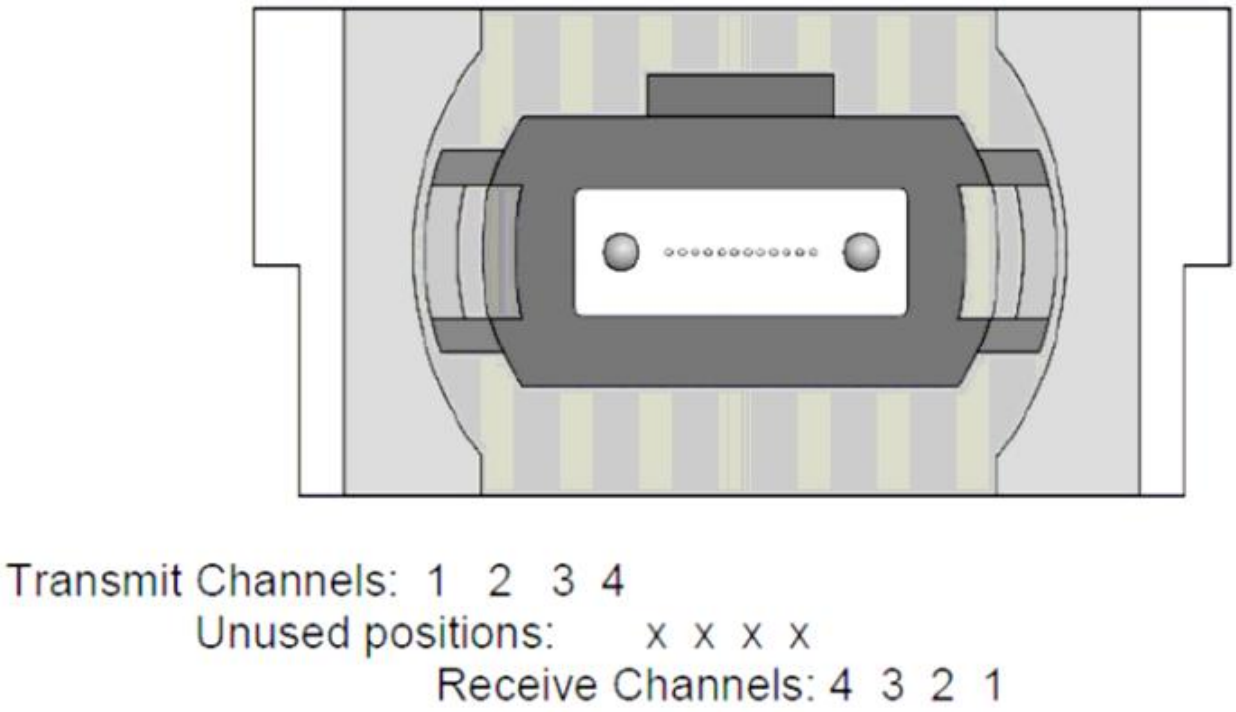

Figure 4. Optical Receptacle and Channel Orientation

DIAGNOSTIC MONITORING INTERFACE

Digital diagnostics functions are available via the I2C interface as specified by CMIS V4.0. The CMIS management memory isshown in Figure 5.

Due to eight-bit addresses, the management memory is divided in Lower Memory (addresses 00h through 7Fh) and Upper Memory (addresses 80h ~ FFh).

The addressing structure of the additional internal management memory is shown in Figure 6. The management memory is arranged as a unique and always host accessible address space of 128 bytes (Lower Memory) and as multiple upper address subspaces of 128 bytes each (Pages), only one of which is selected as host visible in Upper Memory. A second level of Page selection is possible for Pages for which several instances exist (e.g. where a bank of pages with the same Page number exists).

This structure supports a flat 256 byte memory for passive copper modules and permits timely access to addresses in the Lower Memory(e.g. Flags and Monitors). Less time critical entries, e.g. serial ID information and threshold settings, are available with the Page Select function in the Lower Page.

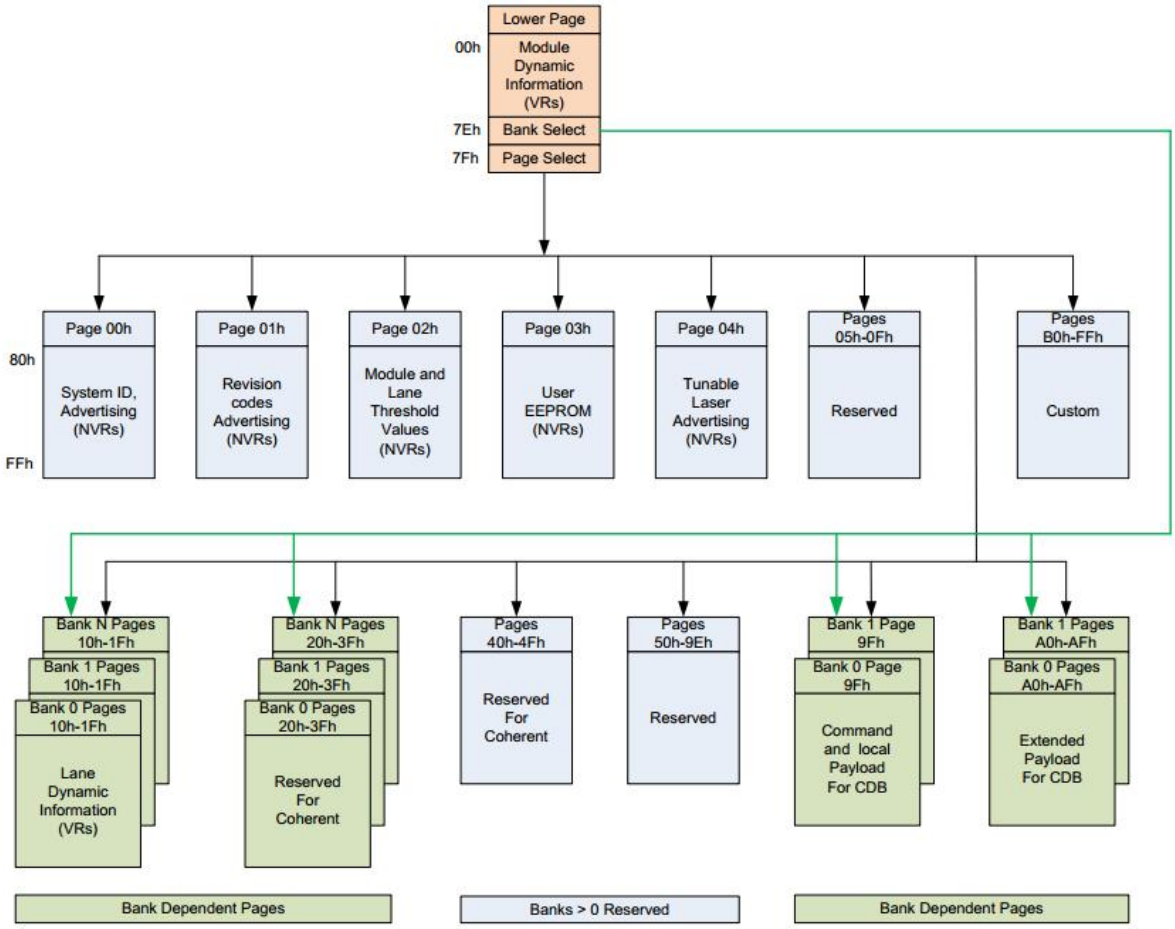

Figure 5.CMIS Bank Page Memory Map

The CMIS memory structure also provides address expansion by adding additional upper pages as needed. Upper pages 00-02 all contain static, non-volatile advertising registers. Upper page 01 provides revision codes and advertising registers that indicate the capabilities of the module. Upper page 02 provides thresholds for monitored functions. Upper page 03 provides a user read/write space.

The lower page, upper pages 00h-03h and bank 0 page 10h-11h aresupported in our module.

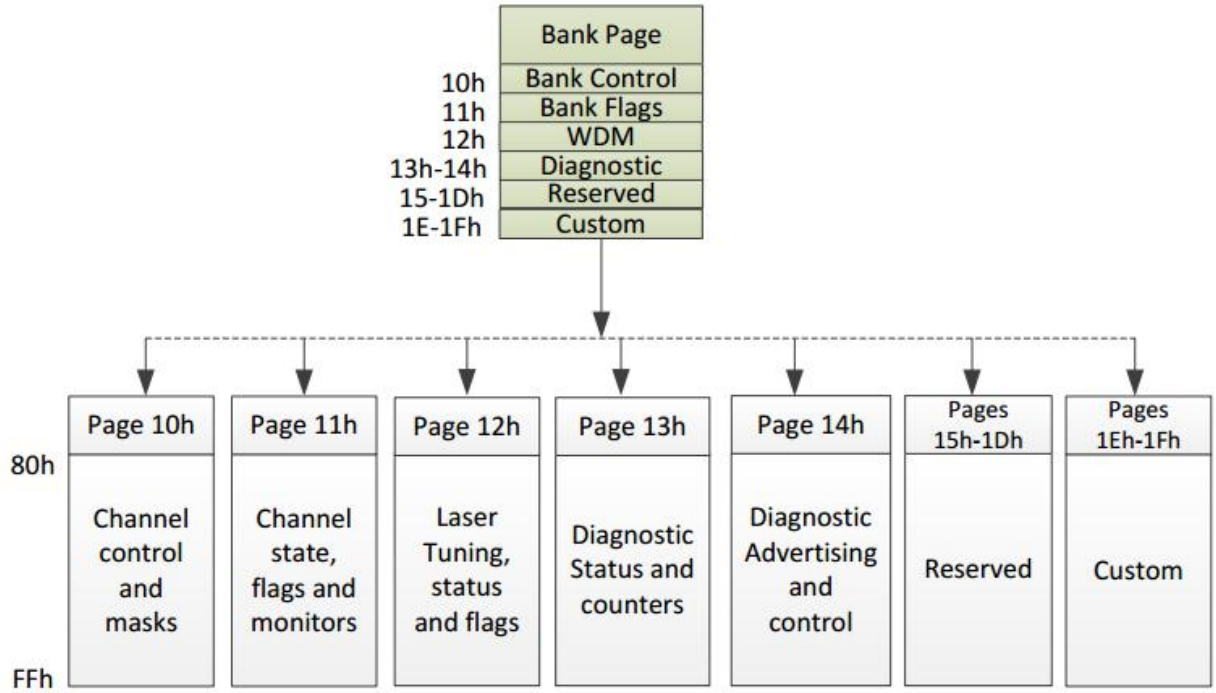

Figure 6.Additional Supported Bank Page Memory Map

The Lower Memory– Page 00h

The Lower Memory consists of the lower 128 bytes of the 256 byte two-wire serial bus addressable space. The Lower Page is used to access a variety of module level measurements, diagnostic functions and controlfunctions, as well as to select which of the various Upper Pages in the structured memory map are accessed bybyte addresses greater or equal than 128.

Address	Size	Subject Area	Description
0–3	4	ID and Status Area	Module ID from SFF-8024 list, version number, Type and status
			Flat mem indication, CLEI present indicator, Maximum TWI speed, Current state of Module, Current state of the Interrupt signal
4–7	4	Lane Flag Summary	Flag summary of all lane flags on pages 10h-1Fh
8-13	6	Module-Level Flags	All flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path specific
26-30	5	Module Global Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Flag Masks	Masking bits for the Module-Level flags
37-38	2	CDB Status Area	Status of most recent CDB command
39-40	2	Module Firmware Version	Module Firmware Version.
41-63	23	Reserved Area	Reserved for future standardization
64-82	19	Custom Area	Vendor or module type specific use
83-84	2	Inactive Firmware Version	Version Number of Inactive Firmware. Values of 00h indicates module supports only a single image.
85-117	33	Application Advertising	Combinations of host and media interfaces that are supported by module data path(s)
118-125	8	Password Entry and Change	
126	1	Bank Select Byte	Bank address of currently visible Page
127	1	Page Select Byte	Page address of currently visible Page

Figure 7.The Lower Memory Overview

The Upper Memory – Page 00h

Upper page 00h contains static read-only module identification information.

Address	Size (bytes)	Name	Description
128	1	Identifier	Identifier Type of module
129-144	16	Vendor name	Vendor name (ASCII)
145-147	3	Vendor OUI	Vendor IEEE company ID
148-163	16	Vendor PN	Part number provided by vendor (ASCII)
164-165	2	Vendor rev	Revision level for part number provided by vendor (ASCII)
166-181	16	Vendor SN	Vendor Serial Number (ASCII)
182-189	8	Date Code	
190-199	10	CLEI code	Common Language Equipment Identification code
200-201	2	Module power characteristics	
202	1	Cable assembly length	
203	1	Media Connector Type	
204-209	6	Copper Cable Attenuation	
210-211	2	Cable Assembly Lane Information	
212	1	Media Interface Technology	
213-220	8	Reserved	
221	1	Custom	
222	1	Checksum	Includes bytes 128-221
223-255	33	Custom Info NV	

Figure 8.Page 00h Memory Overview

The Upper Memory – Page 01h(Advertising)

Upper page 01h contains advertising fields that define properties that are unique to active modules and cable assemblies.

Byte	Size (bytes)	Name	Description
128-131	4	Module Firmware and Hardware revisions	
132-137	6	Supported link length	Supported lengths of various fiber media
138-139	2	Nominal Wavelength	
140-141	2	Wavelength Tolerance	
142-144	3	Implemented Memory Pages and Durations advertising	
145-154	10	Module Characteristics advertising	
155-156	2	Implemented Controls advertising	
157-158	2	Implemented Flags advertising	
159-160	2	Implemented Monitors advertising	
161-162	2	Implemented Signal Integrity Controls advertising	
163-166	4	CDB support advertising	
167-168	2	Additional Durations advertising	
169-175	7	Reserved	
176-190	15	Module Media Lane advertising	
191-222	32	Custom	
223-250	28	Extended Module Host-Media Interface Advertising options	
251-254	4	Reserved	
255	1	Checksum	Checksum of bytes 130-254[1]

Figure 9.Page 01h Memory Overview

The Upper Memory – Page 02h (Module and Lane Thresholds)

Upper Page 02h contains the module-defined thresholds for module-level and lane-specific monitors. The presence ofPage 02h is advertised in bit 7 in Page 00h byte 2.

Byte	Size (bytes)	Name	Description
128-175	48	Module-level monitor thresholds	
176-199	24	Lane-specific monitor thresholds	
200-229	30	Reserved	
230-254	25	Custom	
255	1	Checksum	Covers bytes 128-254

Figure 10.Page 02h Memory Overview

The Upper Memory – Page 10h (Lane and Data Path Control)

The upper memory map page 10h is a banked page that contains lane dynamic control bytes. The presence ofPage 10h is advertised in bit 7 in Page 00h byte 2.

Byte	Size (bytes)	Name	Description
128	1	DataPathDeinit	Data Pathcontrol bits for each lane, controls Data Path State machine
129-142	14	Lane-Specific Control	Fields to control lane attributes independent of the Data Path State machine or control sets
143-177	35	Staged Control Set 0	Fields to configure the selected Application Code and signal integrity settings
178-212	35	Staged Control Set 1	Fields to configure the selected Application Code and signal integrity settings
213-231	19	Lane-Specific Flag Masks	
232-239	8	Reserved	
240-255	16	Custom	

Figure 11.Page 02h Memory Overview

The Upper Memory – Page 11h (Lane Status)

The upper memory map page 11h is a banked page that contains lane dynamic status bytes. The presence of Page 11h is conditional on the state of bit 7 in Page 00h byte 2. All fields on Page 11h are read-only.

Byte	Size (bytes)	Name	Description
128-131	4	Data Path State indicators	
132-133	2	Reserved	
134-152	19	Lane-specific flags	
153	1	Reserved	
154-201	48	Lane-specific monitors	
202-205	4	Configuration Error Codes	Indicates validity of select Application codes
206-234	29	Active Control Set	
235-239	5	Reserved	
240-255	16	Host Electrical to Module Media Lane Mapping	Indicates the mapping of Host Electrical lanes to Module Media lanes

Figure 12.Page 11h Memory Overview

Mechanical Dimensions

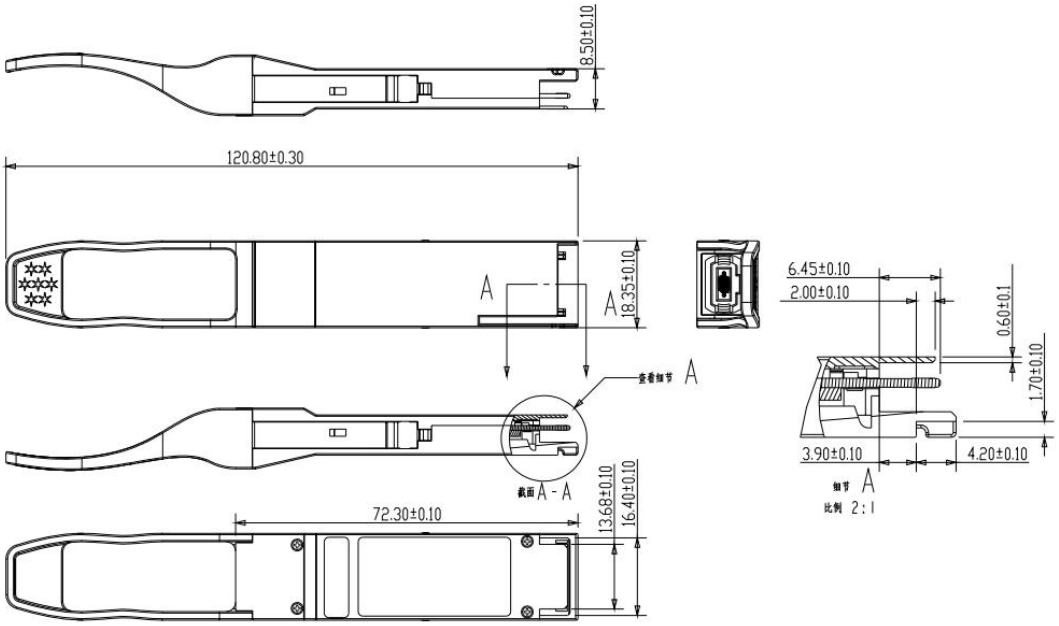

Figure 13. Mechanical Specifications

Regulatory Compliance

GigalightGQS-MPO201-SR4CZCQSFP56 transceiver are Class 1 Laser Products. They are certified per the following standards:

Feature	Standard
Laser Safety	IEC 60825-1:2014 (3rd Edition) IEC 60825-2:2004/AMD2:2010 EN 60825-1-2014 EN 60825-2:2004+A1+A2
Electrical Safety	EN 62368-1: 2014 IEC 62368-1:2014 UL 62368-1:2014
Environmental protection	Directive 2011/65/EU with amendment(EU)2015/863
CE EMC	EN55032：2015 EN55035：2017 EN61000-3-2:2014 EN61000-3-3:2013
FCC	FCC Part 15, Subpart B ANSI C63.4-2014

References

1. QSFP MSA
2. CMISV4.0
3. IEEE 802.3cd200GBASE-SR4 specification

4. Directive 2011/65/EU of the European Parliament and of the Council, “on the restriction of the use of certain hazardous substances in electrical and electronic equipment,” July 1, 2011.

⚠CAUTION:

Use of controls or adjustment or performance of procedures other than those specified herein may result in hazardous radiation exposure.

Ordering Information

Part Number	Product Description
GQS-MPO201-SR4CZC	QSFP56, 200GBASE-SR4 Transceiver, 70m on OM3 (MMF)and 100m on OM4/OM5 MMF, DSP version.

Important Notice

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Revision History

Revision	Date	Description
V0	Sep-5-2022	Advance Release.